UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,142	10/28/2003	Ja Won Seo	2013P112	5530

8791 7590 07/11/2008

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
LE, THI Q	

ART UNIT	PAPER NUMBER
2613	

MAIL DATE	DELIVERY MODE
07/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/696,142	SEO ET AL.	
	Examiner	Art Unit	
	THI Q. LE	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is in response to Applicant's amendment filed on 5/29/2008. **Claims 1-2** are still pending in the present application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1-2** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Smoot (US Patent # 4,565,974)** in view of **Nakamura et al. (US Patent # 5,475,342)** and further in view of **Jarret et al. (France Publication: FR 2532802)** and further in view of **Bayruns et al. (US Patent # 5,602,510)**.

Consider **claim 1**, Smoot clearly shows and discloses, a burst mode optical receiver comprising: a photodiode (read as, photodiode 14; figure 3), which receives an optical signal and converts the optical signal into a current signal (figure 3; column 3 lines 39-40); a pre-amplifier (read as, amplifier 16), which converts the current signal into a voltage signal, amplifies the voltage signal with a gain according to a control signal, and outputs an amplified signal (figure 3; column 1 lines 15-20; and column 3 lines 40-50); a first peak detector (read as, peak-to-peak detector 18), which detects a top peak voltage and a bottom peak voltage of the amplified signal (figure 3; column 3 lines 44-50); and a buffer (read as, buffer stage 42), which buffers an limitedly amplified signal from the first limiting amplifier (figure 3; column 3 lines 54-56).

Smoot fails to disclose; wherein the first peak detector outputs an average value of the detected top peak voltage and the detected bottom peak voltage as a first reference voltage; a first limiting amplifier, which receives the amplified signal and the first reference voltage and amplifies a difference between the amplified signal and the first reference voltage; and Smoot fails to explicitly teach, a gain controller, which compares the first reference voltage with a comparison voltage and outputs the control signal which controls a gain of the pre-amplifier according to the comparison result; and the pre-amplifier comprising an impedance control unit which controls an impedance of the pre-amplifier in response to the control signal and an amplifying unit which converts the current signal into the voltage signal and amplifies the

voltage signal with a gain corresponding to said impedance controlled by the impedance control unit such that when a control signal of a first level is generated from a gain controller a transistor of the impedance control unit is turned on to decrease a trans-impedance of the pre-amplifier and when a control signal of a second level is generated from the gain controller the transistor is turned off to increase the trans-impedance of the pre-amplifier.

However, Smoot teaches a FET shunt device 19, which takes an output result from the differential amplifier and compares it with a BIAS (i.e. predetermined) voltage. The Examiner take official notice, that it is well known in the art that a FET can operate as a variable resistor depending on the potential different between its gate and source. In this case the gate has an input from peak-to-peak detector 18, while the source takes the value of the BIAS voltage; thus depending on the value of the BIAS voltage and peak-to-peak detector 18, the voltage on the drain can vary (figure 3; column 3 lines 45-50). This function provides the function of an automatic gain control.

In related art, Nakamura et al. disclose an amplifier for stably maintaining a constant output. Wherein, the amplifier circuit includes an automatic threshold control circuit (ATC), 10, (read as, first peak detector). The ATC functions such that it detects the top and bottom values of an input waveform and outputs an average value between the top and bottom values. The output of the ATC is use as reference voltage for one of the input of a limiting amplifier, 40 (read as, first limiting amplifier). The original waveform input is use as the second input for the limiting amplifier; and wherein the amplifier produces an output with constant amplitude (figure 4; column 10 lines 8-12; and column 10 lines 34-41).

Smoot disclosed an invention, which achieve the same result as the current application; except for Smoot uses an equalizer amplifier, 26, (Smoot; figure 3) to perform the function of the combination peak detector and limiting amplifier. And Nakamura et al. clearly disclose the use of the combination peak detector and limiting amplifier to achieve the same function as an equalizer amplifier. It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teaching of Nakamura et al. with Smoot. Since, the same function is still achievable if the equalizer amplifier in Smoot's invention is replace with the combination peak detector and limiting amplifier in Nakamura's et al. invention.

Although Smoot does not specifically teaches directly controlling the amplifier's 16 gain based on the measured peak to peak output power level, to obtained a desired output power level; Smoot teaches the use of a FET shunt device 19 to achieve the same function as controlling the gain of the amplifier 16. Discussed on column 4 lines 35-49, the peak to peak detector 18 measure the output voltage level at output node 20; if the peak to peak amplitude is at least a preset threshold value, the FET shunt device 19 is activated. In this manner, the signal voltage amplitude at node 20 is allowed to increase until a predetermined peak to peak amplitude is reached.

In related art, Jarret et al disclose a level control circuit. Wherein, an input optical signal is converted to an electrical signal via PIN diode 21 (figure 2b) and the electrical signal enters a preamplifier 24 (figure 2b). The gain of the preamplifier is controlled by a gain control circuit; wherein the gain control circuit comprises a filter and a peak to peak detector. Gain control is performed by comparing the amplified electrical signal with a reference signal and adjusting the gain of the preamplifier according to the comparison result.

It would have been obvious for a person of ordinary skill in the art at the time of the invention to substitute the level control circuit of Jarret et al with that disclosed by Smoot. Since, Jarret et al and Smoot is trying to achieve the same goal (i.e. adjusting the output signal level from the preamplifier according to the comparison result of the peak to peak value with a reference value. Thus, the two circuits provide by Jarret et al and Smoot are equivalent.

In related art, Bayruns et al. clearly disclose an automatic transimpedance control amplifier having a variable impedance feedback. Wherein, the transimpedance amplifier comprises a plurality of variable resistance means, each means having first, second, and control terminals (read as, impedance control unit), the resistance between the first and second terminals being variable by applying an electronic signal to the control terminal. Additionally, each said variable resistance means is connected between the output node of one voltage gain stage (read as, amplifying unit) and the input node of the first stage, with the first terminal of the variable resistance means being connected to the output node of the one stage, and the second terminal being connected to the input node of the first gain stage, whereby a voltage gain of the one stage being controlled by changing the resistance of the variable resistive means (abstract; column 2 lines 29-42). Further, Bayruns discloses, when a control signal of a first level is generated from a gain controller a transistor of the impedance control unit is turned on to decrease a trans-impedance of the pre-amplifier and when a control signal of a second level is generated from the gain controller the transistor is turned off to increase the trans-impedance of the pre-amplifier (figure 2 shows, changing the source-to-drain resistance of MAGC1 (transistor) changes the voltage gain of the second stage. Hence it can be understood that, by controlling the MAGCI 1 the voltage gain can be adjusted accordingly; figure 2, column 5 lines 15-37).

Although Smoot as modified by Nakamura et al. and Jarret et al, disclosed the use of variable game amplifier, he fails to disclose the structure and method of how the gain of the variable gain amplifier can be change. Bayruns et al. disclosed the structure plus the methods of changing the gain for a variable gain amplifier. Thus, It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teaching of Smoot as modified by Nakamura et al. with Bayruns et al. Because Bayruns et al. disclosed one particular structure and method of which the gain of a variable gain amplifier can be affected.

Consider **claim 2, and as applied to claim 1 above**, Smoot as modified by Nakamura et al. further disclose; a second peak detector (read as, automatic threshold control circuit (ATC), 10, within each basic circuit BC1-BCn; Nakamura et al., figure 6), which detects a top peak voltage and a bottom peak voltage of the limitedly amplified signal and outputs an average value of the detected top peak voltage and the detected bottom peak voltage as a second reference voltage; and a second limiting amplifier (read as, limiting amplifier, 4, within each basic circuit BC1-BCn; Nakamura et al., figure 6), which receives the limitedly amplified signal and the second reference voltage, amplifies the difference between the limitedly amplified signal and the second reference voltage, and outputs an amplified signal to the buffer (Nakamura et al.; figure 6; column 12 lines 22-35).

Conclusion

for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450

Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thi Le whose telephone number is (571) 270-1104. The Examiner can normally be reached on Monday-Friday from 7:30am to 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Thi Le

/Kenneth N Vanderpuye/
Supervisory Patent Examiner, Art Unit 2613

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/696,142	SEO ET AL.	
	Examiner	Art Unit	
	THI Q. LE	2613	